REMARKS

The Examiner rejected claims 1-39 as obvious over U.S. Patent No. 6,154,475 to Soref et al. ("Soref") in view of U.S. Patent No. 5,166,084 to Pfiester ("Pfiester"). Applicants hereby cancel claims 2, 4, 6-9, 19, 21, 24-25, 27-31, 35, and 37-39 mooting this rejection with respect to these claims. Applicants respectfully traverse this rejection of claims 1, 3, 5, 10-18, 20, 22-23, 26, 32-34, and 36 to the extent is maintained against the claims, as amended.

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. M.P.E.P. §2143.03, *citing*, In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). Moreover, in determining the differences between the prior art and the claims, the question under 35 U.S.C. § 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. M.P.E.P. § 2141.02, *citing*, Stratoflex, Inc. v. Aeroquip Corp., 713 F.3d 1530 (Fed. Cir. 1983); Schenk v. Nortron Corp., 713 F.2d 782 (Fed. Cir. 1983). Similarly, a prior art reference also must be considered in its entirety, *i.e.*, as a whole, including portions that would lead away from the claimed invention. M.P.E.P. § 2141.02, *citing*, W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984).

Independent claim 1, as amended, recites a method of fabricating a semiconductor device that includes the steps of chemically reacting at least a portion of a $Si_{1-y}Ge_y$ layer to form a chemically modified $Si_{1-y}Ge_y$ layer on a strained channel layer and removing said chemically modified $Si_{1-y}Ge_y$ layer to expose said strained channel layer.

Neither Soref nor Pfiester teach or suggest the invention recited by independent claim 1, as amended, at least because neither reference describes a method for making a semiconductor device in which a sacrificial $Si_{1-y}Ge_y$ layer is chemically reacted in order to form a chemically modified sacrificial $Si_{1-y}Ge_y$ layer on a strained channel layer that is subsequently removed to expose the strained channel layer. Soref is directed a family of lasers having a highly-doped, stably-strained SiGe or Ge collector layer formed on a SiGe graded relaxed buffer layer. Soref discloses no novel fabrication techniques and nowhere suggests the step of chemically reacting a sacrificial $Si_{1-y}Ge_y$ layer to form a chemically modified $Si_{1-y}Ge_y$ layer on a strained channel layer, as explicitly recited by independent claim 1.

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Pfiester is directed to a process for fabricating a Silicon-on-Insulator Field Effect Transistor. A SiGe layer is used to form the source and drain current electrodes, and part of the SiGe layer is etched so that gate material can be deposited where the SiGe layer is removed (see Pfiester, Figs. 1A-4). Although Pfiester discloses etching a portion of the SiGe layer, it does not teach or suggest that chemically reacting a sacrificial SiGe layer to form a chemically modified $Si_{1-y}Ge_y$ on a strained channel layer, as explicitly recited by independent claim 1.

Since neither Soref nor Pfiester teach or suggest all the limitations of independent claim 1, as amended, and claims 3, 5, 10-18 and 40-41 that depend either directly or indirectly from claim 1, Applicants respectfully submit that the rejection of those claims as obvious in view of Soref and Pfiester is overcome and should be withdrawn.

Moreover, Applicants respectfully submit that neither Soref nor Pfiester teach or suggest the invention recited in independent claims 20 and 36, as amended. Independent claims 20 and 36, as amended, recite a method of fabricating a semiconductor device that includes the step of removing a SiGe layer to expose the underlying layer. As noted above, Soref is directed a family of lasers having a highly-doped, stably-strained SiGe or Ge collector layer formed on a SiGe graded relaxed buffer layer. Soref discloses no novel fabrication techniques.

Pfiester is directed to a process for fabricating a Silicon-on-Insulator Field Effect Transistor. A SiGe layer is used to form the source and drain current electrodes, and part of the SiGe layer is etched so that gate material can be deposited where the SiGe layer is removed (see Pfiester, Figs. 1A-1D). Although Pfiester discloses etching a portion of the SiGe layer, it does not teach or suggest that the entire sacrificial SiGe layer should be etched to expose the strained channel layer, as explicitly recited by independent claim 20, or the Si layer, as explicitly recited by independent claim 36. Pfiester invention, as a whole, requires that the SiGe layer is selectively etched, because the remaining SiGe material forms the source and drain electrodes for the Pfiester device.

Thus, Applicants respectfully submit that the invention of amended claims 20 and 36, as a whole, is not suggested by Soref or Pfiester, either alone or in proper combination.

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Since neither Soref nor Pfiester teach or suggest all the limitations of independent claims 20 and 36, as amended, and claims 22-23, 26, 32-34 and 42-44 that depend either directly or indirectly therefrom, Applicants respectfully submit that the rejection of those claims as obvious in view of Soref and Pfiester is overcome and should be withdrawn.

CONCLUSION

Applicants request that the Examiner reconsider the application and claims in light of the foregoing Amendment and Response. If, in the Examiner's opinion, a telephonic interview would expedite the favorable prosecution of the present application, the undersigned attorney would welcome the opportunity to discuss any outstanding issues, and to work with the Examiner toward placing the application in condition for allowance.

Respectfully submitted,

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MARKED-UP VERSION OF THE CLAIMS AS AMENDED

1. (Amended) A method of fabricating a semiconductor device comprising:

(a) providing a semiconductor heterostructure[, said heterostructure] comprising a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a strained channel layer on said relaxed $Si_{1-x}Ge_x$ layer, and a $Si_{1-y}Ge_y$ layer on said strained channel layer;

(b) [removing] chemically reacting at least a portion of said $Si_{1-y}Ge_y$ layer to form a chemically modified $Si_{1-y}Ge_y$ layer on said strained channel layer;

(c) removing said chemically modified $Si_{1-y}Ge_y$ layer to expose said strained channel layer; and

(d) providing a dielectric layer on said exposed strained channel layer.

2. (Cancelled)

3. (Amended) The method of claim 1[2,] wherein step (b) comprises oxidizing said at least a portion of said $Si_{1-y}Ge_y$ layer [said selective technique is wet oxidation below 750C].

4. (Cancelled)

5. (Amended) The method of claim 1 wherein said dielectric layer comprises a gate dielectric of a MISFET.

6. (Cancelled)

7. (Cancelled)

8. (Cancelled)

9. (Cancelled)

10. (Amended) The method of claim 1 wherein the strained channel layer comprises Si.

11. (Amended) The method of claim 1 wherein x is approximately equal to y.

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12. (Amended) The method of claim 11 wherein step (a) further [comprising] comprises providing a sacrificial Si layer on said [sacrificial] $Si_{1-y}Ge_y$ layer.

13. (Amended) The method of claim 1 wherein $y > x$.

14. (Amended) The method of claim 13 wherein step (a) further [comprising] comprises providing a sacrificial Si layer on said [sacrificial] $Si_{1-y}Ge_y$ layer.

15. (Amended) The method of claim 14 wherein step (a) further comprises providing a [the thickness of the] sacrificial Si layer on said $Si_{1-y}Ge_y$ layer having a thickness [is] greater than the critical thickness.

16. (Amended) The method of claim 1 wherein said substrate comprises Si.

17. (Amended) The method of claim 1 wherein said substrate comprises Si having [with] a layer of SiO_2 thereon.

18. (Amended) The method of claim 1 wherein said substrate comprises a SiGe graded buffer layer on Si.

19. (Cancelled)

20. (Amended) A method of fabricating a semiconductor device comprising:

(a) providing a semiconductor heterostructure[, said heterostructure] comprising a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a strained channel layer on said relaxed $Si_{1-x}Ge_x$ layer, and a $Si_{1-y}Ge_y$ layer on said strained channel layer;

(b) removing said $Si_{1-y}Ge_y$ layer to expose said strained channel layer;

[removing a portion of said strained channel layer to eliminate any residual Ge;] and

(c) providing a dielectric layer on said exposed strained channel layer.

21. (Cancelled)

22. (Amended) The method of claim 20 wherein step (c) comprises forming [said dielectric layer comprises] the gate dielectric of a MISFET by providing a dielectric layer on said exposed strained channel layer.

23. (Amended) The method of claim 22 wherein step (c) comprises forming the gate dielectric of a MISFET by providing an oxide on said exposed strained channel layer [the gate dielectric comprises an oxide].

24. (Cancelled)

25. (Cancelled)

26. (Amended) The method of claim 20 wherein said strained channel comprises Si.

27. (Cancelled)

28. (Cancelled)

29. (Cancelled)

30. (Cancelled)

31. (Cancelled)

32. (Amended) The method of claim 20 wherein said substrate comprises Si.

33. (Amended) The method of claim 20 wherein said substrate comprises Si [with] having a layer of SiO_2 thereon.

34. (Amended) The method of claim 20 wherein said substrate comprises a SiGe graded buffer layer on Si.

35. (Cancelled)

36. (Amended) A method of fabricating a semiconductor device comprising the steps of:

(a) providing a semiconductor heterostructure[, said heterostructure] comprising a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a strained channel layer on said relaxed $Si_{1-x}Ge_x$ layer, a $Si_{1-y}Ge_y$ spacer layer, a Si layer, and a $Si_{1-w}Ge_w$ layer;

(b) removing said $Si_{1-w}Ge_w$ layer to expose said Si layer; and

(c) providing a dielectric layer on said Si layer.

37. (Cancelled)

38. (Cancelled)

39. (Cancelled)

40. (New) The method of claim 3 wherein oxidizing of at least a portion of said $Si_{1-y}Ge_y$ layer is performed using a wet oxidation technique.

41. (New) The method of claim 40 wherein said wet oxidation technique is utilized at a temperature up to about 750°C.

42. (New) The method of claim 20 wherein step (b) comprises removing said $Si_{1-y}Ge_y$ layer to expose said strained channel layer using either wet or dry etch technique.

43. (New) The method of claim 20 further comprising the step of removing at least a portion of the strained channel layer to eliminate residual Ge.

44. (New) The method of claim 36 wherein step (b) comprises removing said $Si_{1-w}Ge_w$ layer to expose said Si layer using either wet or dry etch technique.

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